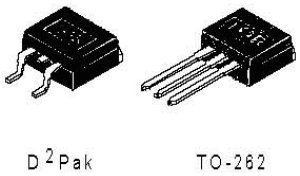
IRFZ48S/L
HEXFET ® Power MOSFET

Advanced Process Technology
Surface Mount (IRFZ48S)
Low-profile through-hole (IRFZ48L)
175°C Operating Temperature
Fast Switching

V_{DSS}=60V
$R_{DS(on)}$=0.018Ω
I_D=50A ⑥



D²Pak TO-262

Description

Third Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device for use in a wide variety of applications.

The D^2Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides he highest power capability and the lowest possible on-resistance in any existing surface mount package. The D^2Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application. The through-hole version (IRFZ48L) is available for low-profile applications.

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D@Tc=25°C	Continuous Drain Current, V_{GS} @ 10V ⑤	50⑥	A
I_D@Tc=100°C	Continuous Drain Current, V_{GS} @ 10V ⑤	50⑥	
I_{DM}	Pulsed Drain Current ①⑤	290	
P_D@ T_A=25°C	Power Dissipation	3.7	W
P_D@Tc=25°C	Power Dissipation	190	W
	Linear Derating Factor	1.3	W/°C
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy ②⑤	100	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑤	4.5	V/nS
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +175	°C
	Soldering Temperature, for 10 seconds	300 (1.6MM from case)	

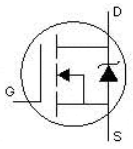
Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\Theta JC}$	Junction-to-Case	-	0.80	°C/W
R_{QJA}	Junction-to-Ambient (PCB Mounted, steady-state)**	-	4	

Electrical Characteristics @ TJ=25 (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	60	-	-	V	V_{GS}=0V, I_D=250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	-	0.06	-	V/°C	Reference to 25°C, I_D=1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	-	-	0.018	Ω	V_{GS}=10V, I_D=43A④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	-	4.0	V	V_{DS}=V_{GS},I_D=250μA
gfs	Forward Transconductance	27	-	-	S	V_{DS}=25V, I_D=43A ⑤
I_{DSS}	Drain-to-Source Forward Leakage	-	-	25	μA	V_{DS}=60V, V_{GS}=0V
		-	-	100		V_{DS}=48V, V_{GS}=0V, T_J=150°C
I_{GSS}	Gate-to-Source Forward Leakage	-	-	100	nA	V_{GS}=20V
	Gate-to-Source Reverse Leakage	-	-	-100		V_{GS}=-20V
Qg	Total Gate Charge	-	-	110	nC	I_D=72A
Qgs	Gate-to-Source Charge	-	-	29		V_{DS}=48V
Qgd	Gate-to-Drain (“Miller”) Charge	-	-	36		V_{GS}=10V, See Fig. 6 and 13 ④⑤
td(on)	Turn-On Delay Time	-	8.1	-	ns	V_{DD}=30V
tr	Rise Time	-	250	-		I_D=72A
td(off)	Turn-Off Delay Time	-	210	-		R_G=9.1Ω
tf	Fall Time	-	250	-		R_D=0.35Ω, See Fig. 10④
Ls	Internal Source Inductance	-	7.5	-	nH	Between lead, And center of die contact
Ciss	Input Capacitance	-	2400	-	pF	V_{GS}=0V
Coss	Output Capacitance	-	1300	-		V_{DS}=25V
Crss	Reverse Transfer Capacitance	-	190	-		f=1.0MHz, See Fig. 5 ⑤

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	-	-	50①	A	MOSFET symbol showing the intergral reverse p-n junction diode 
I_{SM}	Pulsed Source Current (Body Diode) ①	-	-	290		
V_{SD}	Diode Forward Voltage	-	-	2.0	V	T_J=25°C, I_S=72A, V_{GS}=0V④
T_{rr}	Reverse Recovery Time	-	120	180	ns	TJ=25°C, IF=72A
Q_{rr}	Reverse Recovery Charge	-	500	800	nC	di/dt =100A/μs ④⑤
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+ L_D)				

Notes:

①Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

②V_{DD}=25V, starting T_J=25°C, L=22μH, R_G=25Ω, I_{AS}=72A. (See Figure 12)

③I_{SD}≤72A, di/dt ≤200A/μs, V_{DD}≤$V_{(BR)DSS}$, T_J≤175°C

④Pulse width ≤300μs; duty cycle ≤2%.

⑤Uses IRFZ48 data and test conditions

⑥Calculated continuous current based on maximum allowable junction temperature; for recommended current-handing of the package refer to Design Tip # 93-4

**When mounted on 1” square PCB (FR-4 or G-10 Material).

For recommended footprint and soldering techniques refer to application note # AN-994.

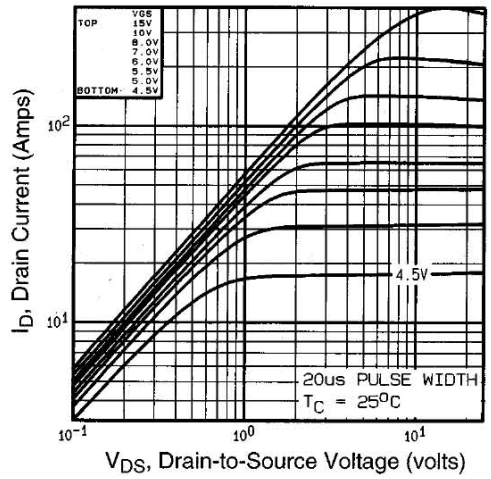


Fig 1. Typical Output Characteristics,

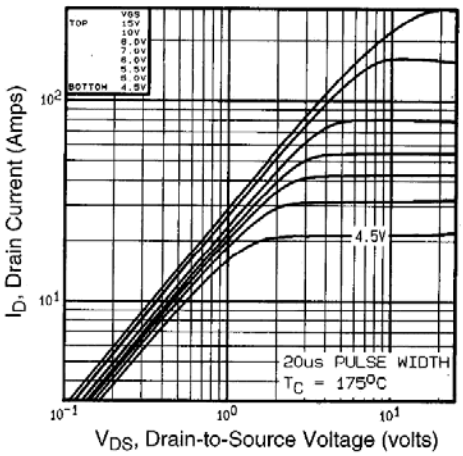


Fig 2. Typical Output Characteristics,

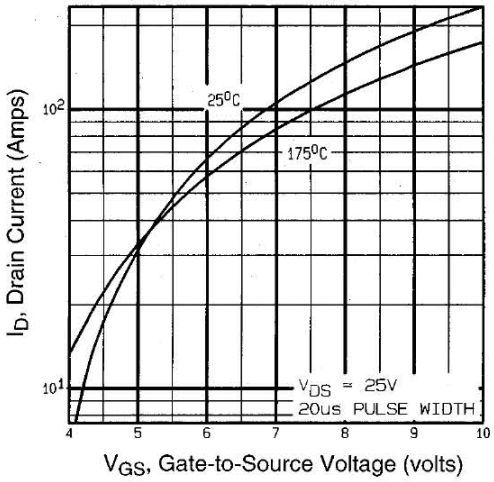


Fig 3. Typical Transfer Characteristics

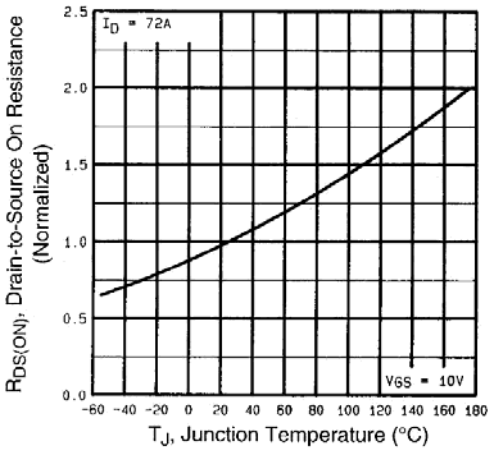


Fig 4. Normalized On-Resistance
Vs. Temperature

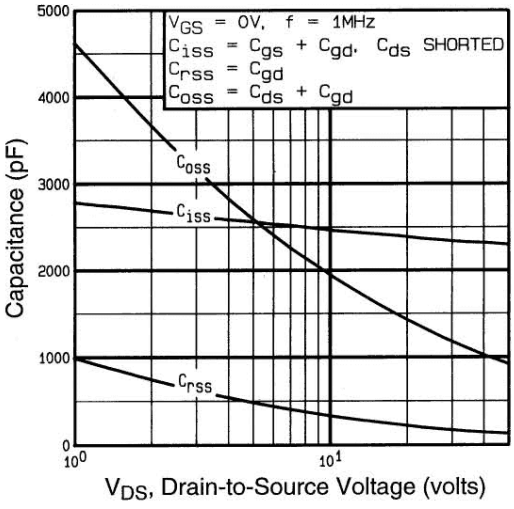


Fig 5. Typical Capacitance Vs.
Drain-to-Source Voltage

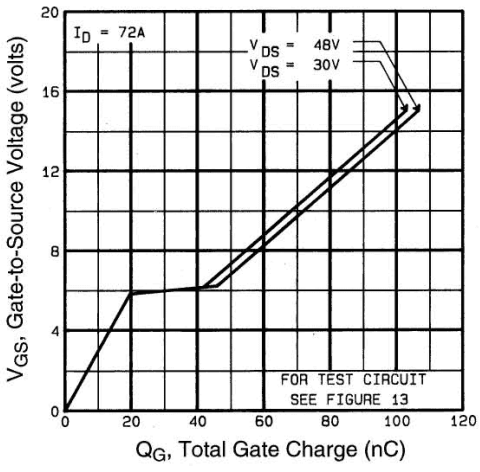


Fig 6. Typical Gate Charge Vs.
Gate-to-Source Voltage

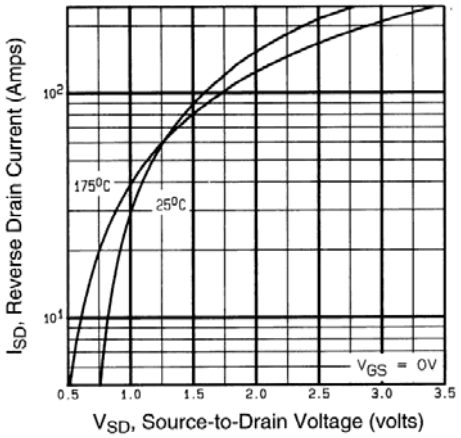


Fig 7. Typical Source-Drain Diode Forward Voltage

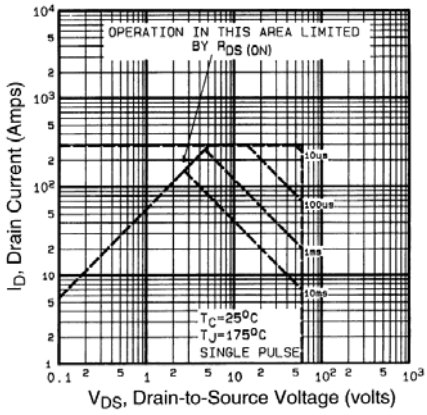


Fig 8. Maximum Safe Operating Area

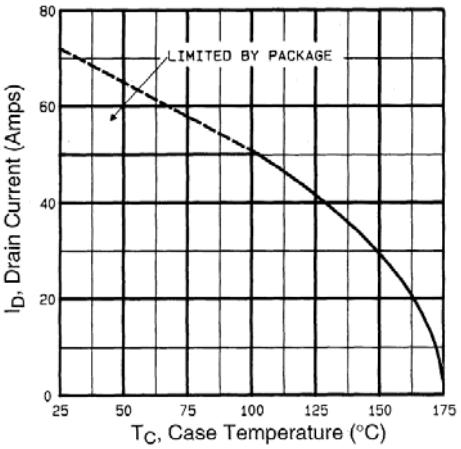


Fig 9. Maximum Drain Current Vs. Case Temperature

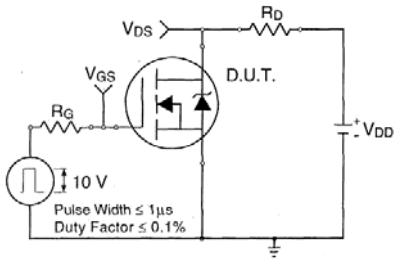


Fig 10a. Switching Time Test Circuit

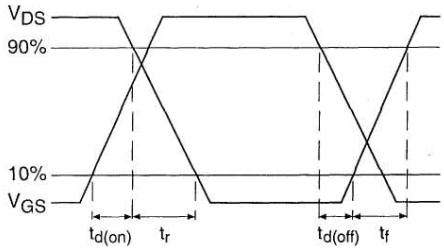


Fig 10b. Switching Time Waveforms

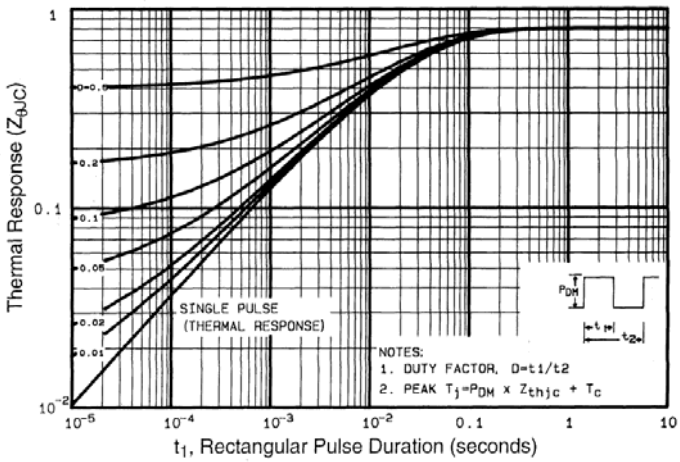


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

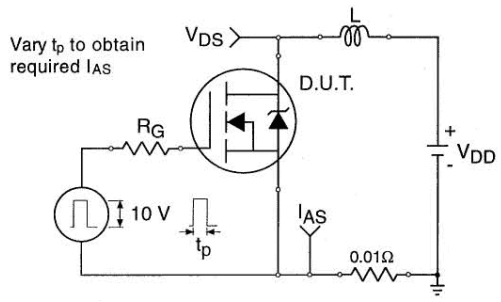


Fig 12a. Unclamped Inductive Test Circuit

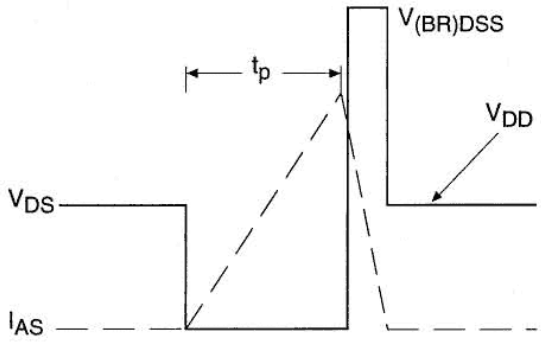


Fig 12b. Unclamped Inductive Waveforms

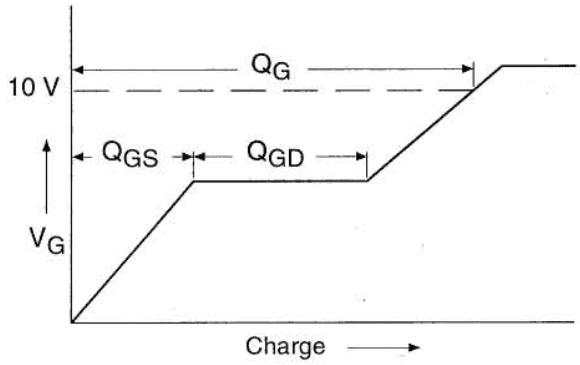


Fig 13a. Basic Gate Charge Waveform

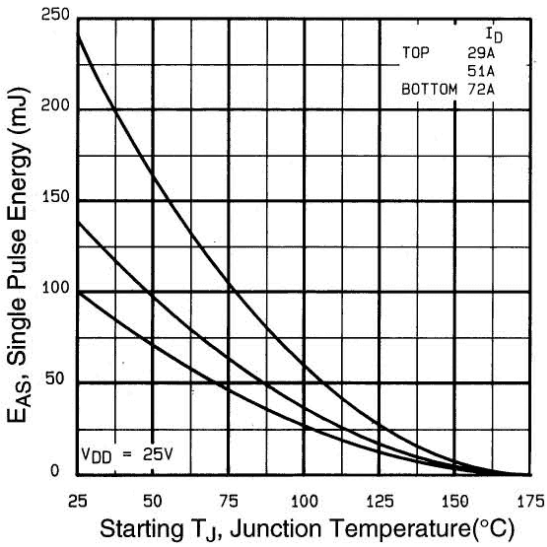


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

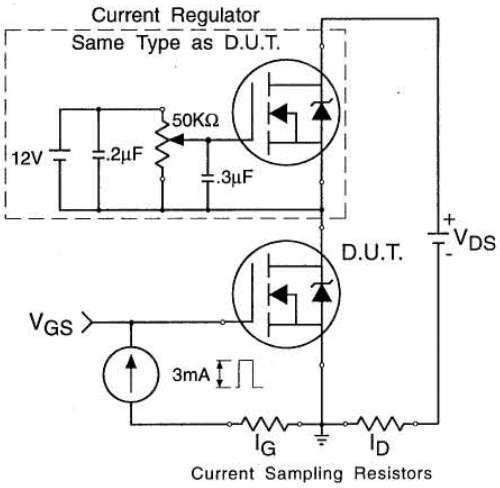
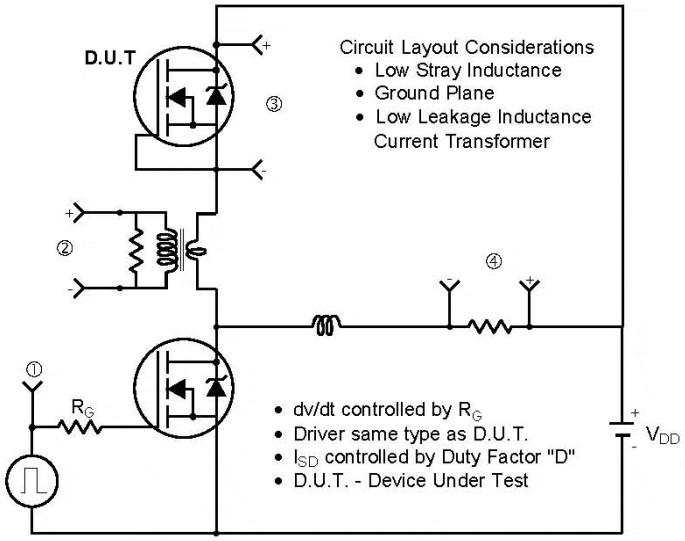
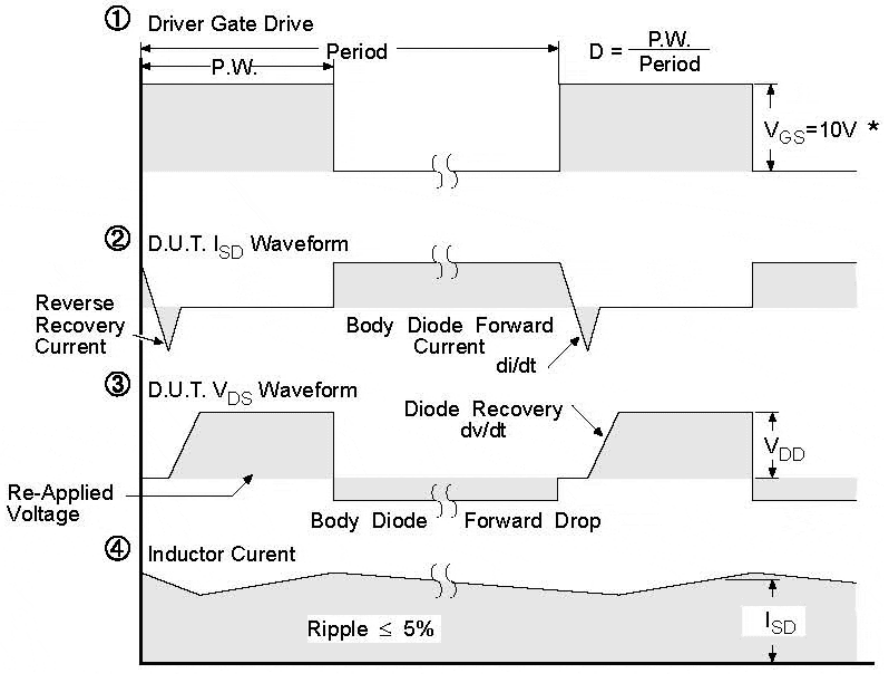


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit

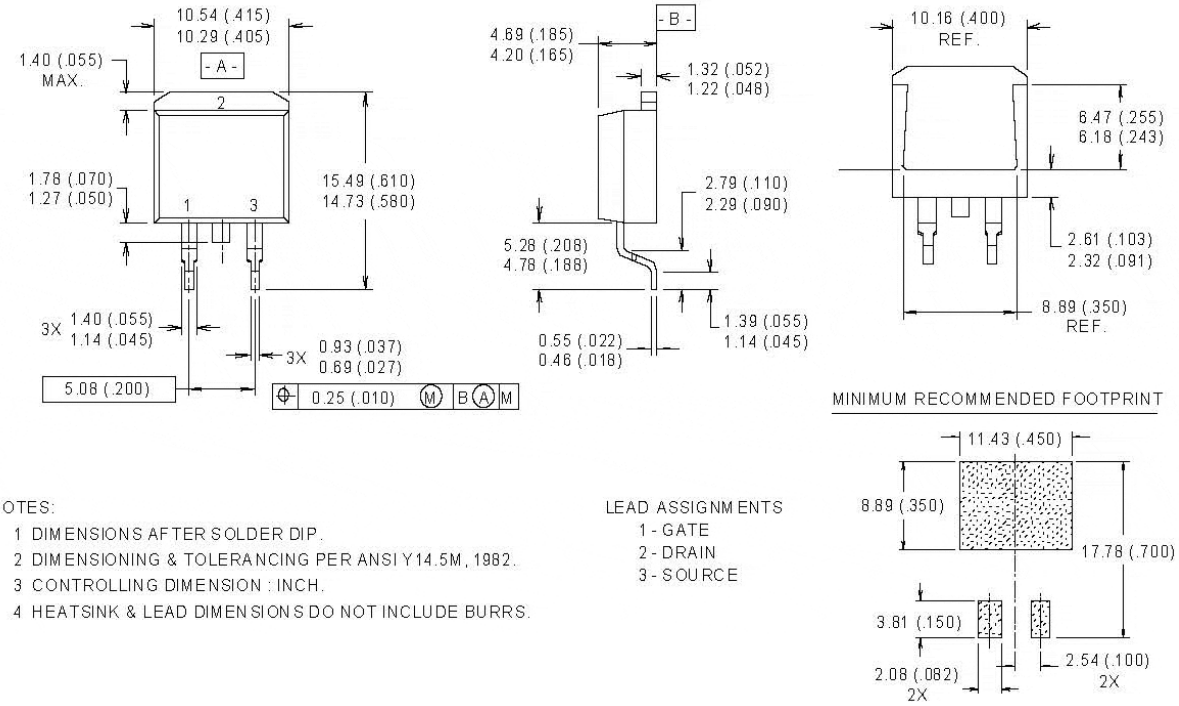




* V_{GS} = 5V for Logic Level Devices

Fig 14. For N-Channel HEXFETS

D^{2}Pak Package Outline



NOTES:

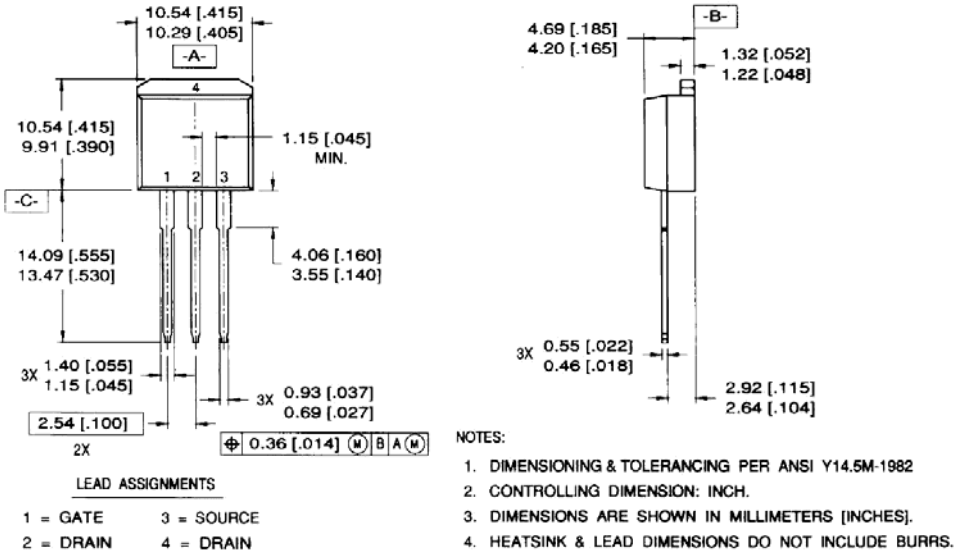
1 DIMENSIONS AFTER SOLDER DIP.
2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
3 CONTROLLING DIMENSION : INCH.
4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

LEAD ASSIGNMENTS

1 - GATE
2 - DRAIN
3 - SOURCE

Package Outline

TO-262 Outline



Tape & Reel Information

D^2Pak